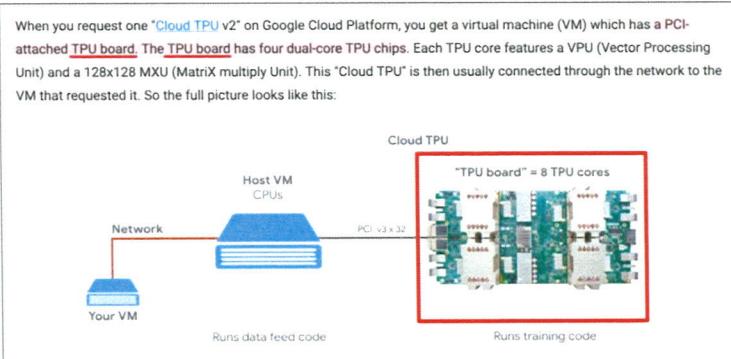
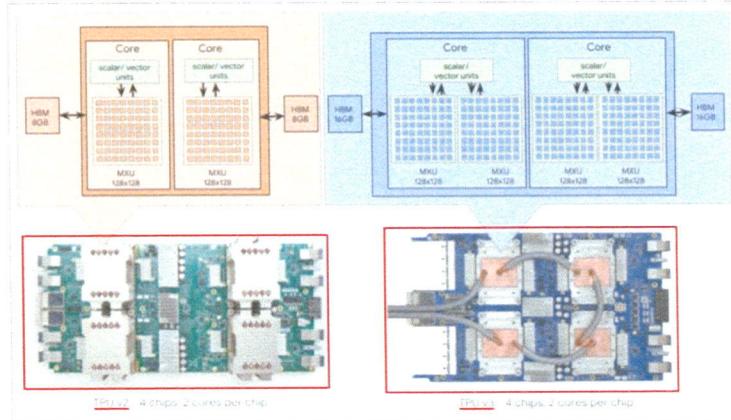


EXHIBIT H

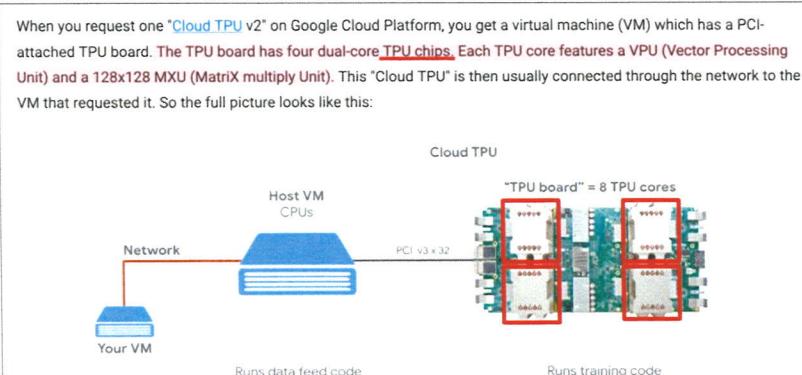
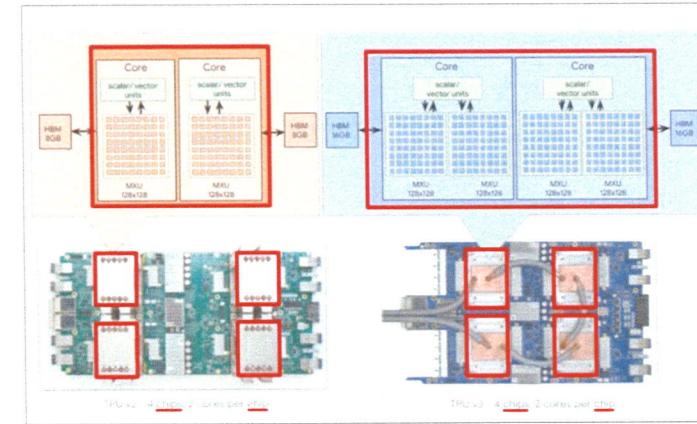
Exhibit A

U.S. Pat. No. 9,218,156

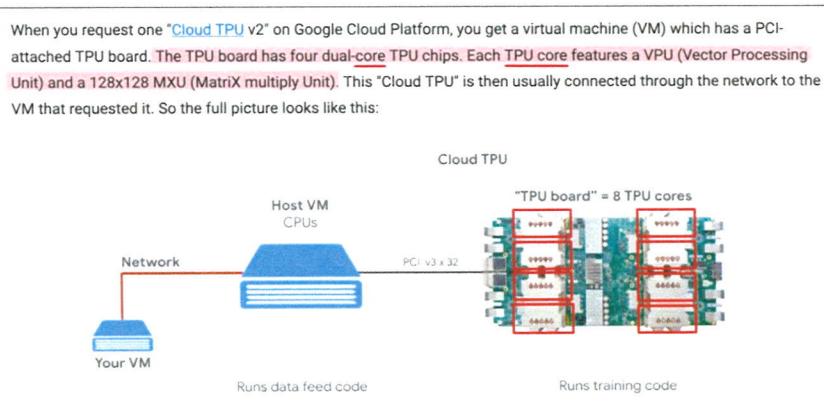
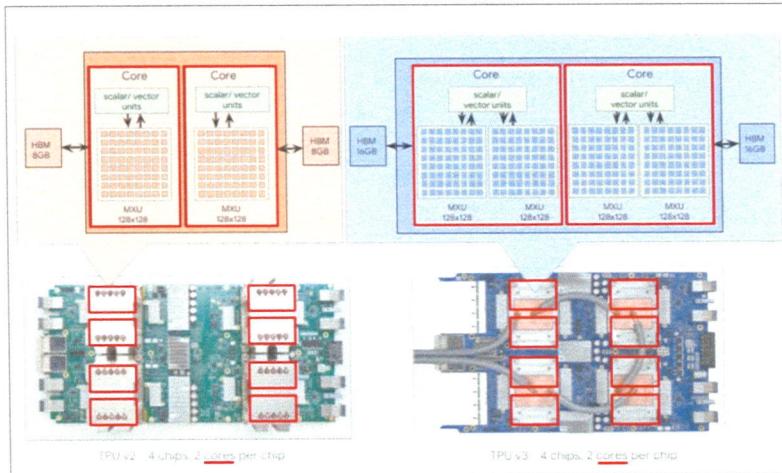
Claim 7

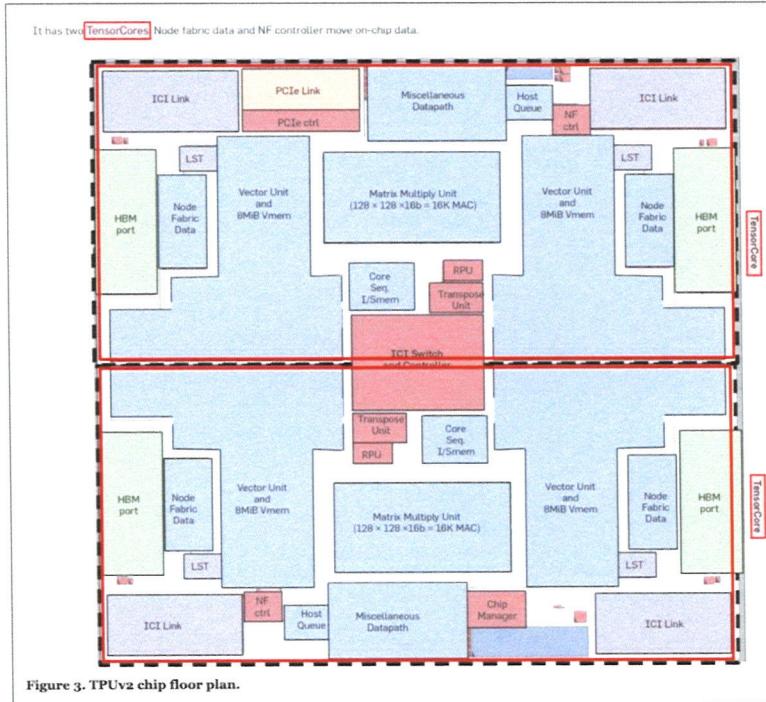
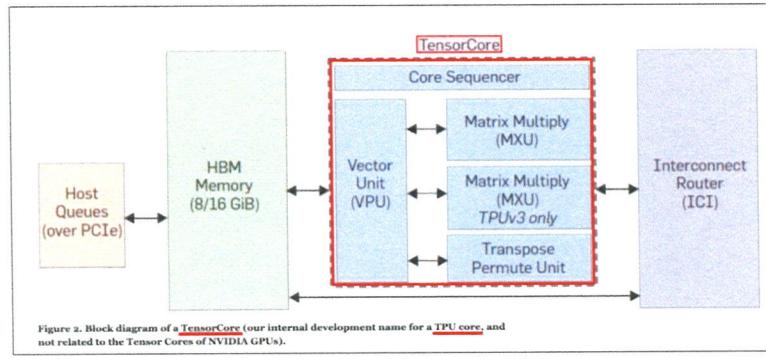
'156 PATENT	INFRINGEMENT EVIDENCE
<p>7. A device comprising:</p> <p>at least one first low precision high-dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value,</p> <p>wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=5% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X% of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.05% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input;</p> <p>at least one first computing device adapted to control the operation of the at least one first LPHDR execution unit</p> <p>wherein the at least one first computing device comprises at least one of a central processing unit (CPU), a graphics processing unit (GPU), a field programmable gate array (FPGA), a microcode-based processor, a hardware sequencer, and a state machine; and,</p> <p>wherein the number of LPHDR execution units in the device exceeds by at least one hundred the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide.</p>	<p>As demonstrated below, the Accused Products include multiple components that, separately and independently, meet all the requirements of the claimed “device.” For example, a “TPU Board” satisfies these requirements:</p> <div style="border: 1px solid black; padding: 10px;"> <p>When you request one “Cloud TPU v2” on Google Cloud Platform, you get a virtual machine (VM) which has a PCI-attached <u>TPU board</u>. The <u>TPU board</u> has four dual-core TPU chips. Each TPU core features a VPU (Vector Processing Unit) and a 128x128 MXU (Matrix multiply Unit). This “Cloud TPU” is then usually connected through the network to the VM that requested it. So the full picture looks like this:</p>  <p>Illustration: your VM with a network-attached “Cloud TPU” accelerator. “The Cloud TPU” itself is made of a VM with a PCI-attached <u>TPU board</u> with four dual-core TPU chips on it.</p> <p>https://codelabs.developers.google.com/codelabs/keras-flowers-convnets/#2</p>  <p>https://cloud.google.com/tpu/docs/system-architecture</p> </div>

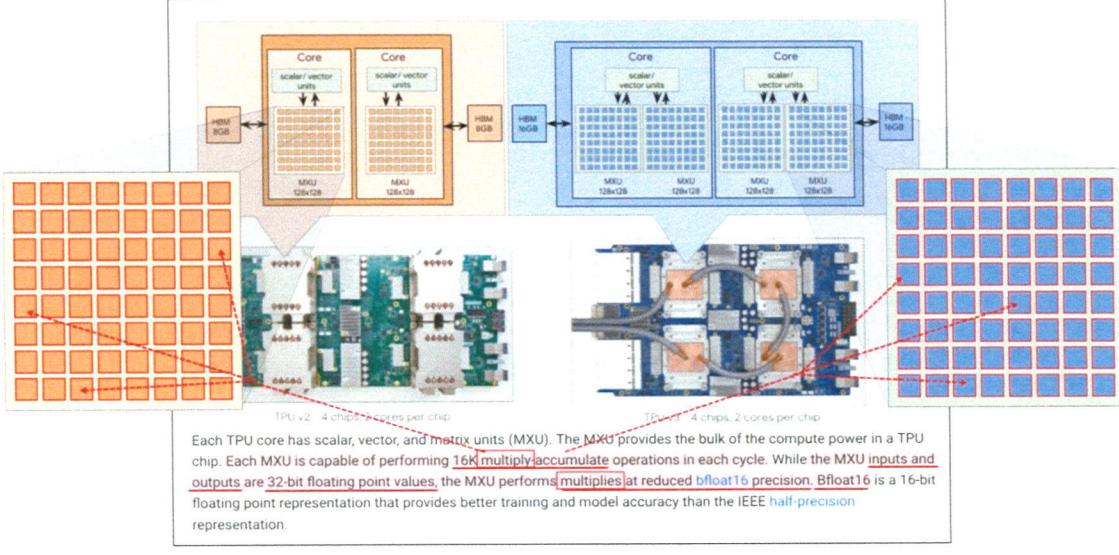
¹ Unless indicated otherwise, color-coded annotations have been added in order to identify relevant components and features of the Accused Products.

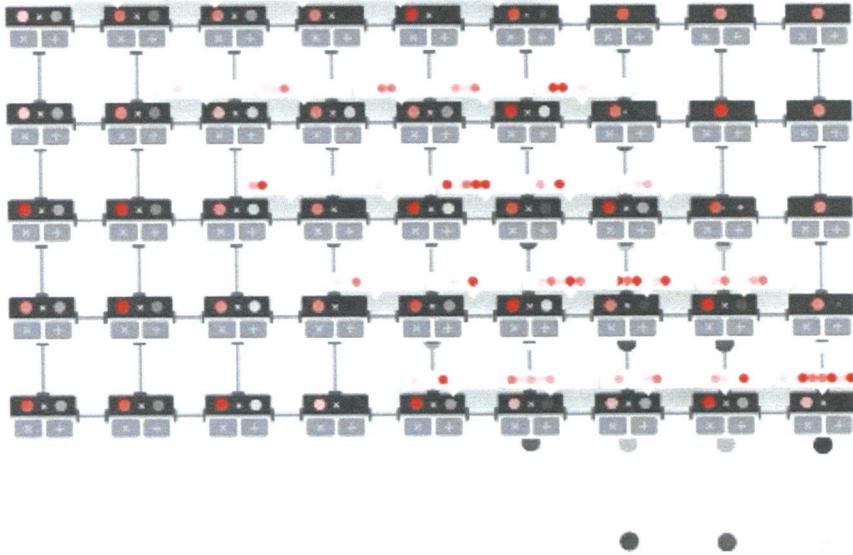
'156 PATENT	INFRINGEMENT EVIDENCE
<p>7. A <u>device</u> comprising:</p> <p>at least one first low precision high-dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value,</p> <p>wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=5% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X% of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.05% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input;</p> <p>at least one first computing device adapted to control the operation of the at least one first LPHDR execution unit</p> <p>wherein the at least one first computing device comprises at least one of a central processing unit (CPU), a graphics processing unit (GPU), a field programmable gate array (FPGA), a microcode-based processor, a hardware sequencer, and a state machine; and,</p> <p>wherein the number of LPHDR execution units in the device exceeds by at least one hundred the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide.</p>	<p>As demonstrated below, the Accused Products include multiple components that, separately and independently, meet all the requirements of the claimed “device.” For example, a “TPU Chip” satisfies these requirements:</p> <div style="border: 1px solid black; padding: 10px; margin-bottom: 10px;"> <p>When you request one Cloud TPU v2 on Google Cloud Platform, you get a virtual machine (VM) which has a PCI-attached TPU board. The TPU board has four dual-core <u>TPU chips</u>. Each TPU core features a VPU (Vector Processing Unit) and a 128x128 MXU (Matrix multiply Unit). This “Cloud TPU” is then usually connected through the network to the VM that requested it. So the full picture looks like this:</p>  <p>Cloud TPU</p> <p>Host VM CPUs</p> <p>Network</p> <p>PCI v3 x 32</p> <p>"TPU board" = 8 TPU cores</p> <p>Runs data feed code</p> <p>Runs training code</p> <p>Illustration: your VM with a network-attached "Cloud TPU" accelerator. The Cloud TPU itself is made of a VM with a PCI-attached TPU board with <u>four dual-core TPU chips</u> on it.</p> </div> <p>https://codelabs.developers.google.com/codelabs.keras-flowers-convnets/#22</p>  <p>TPUv2 - 4 chips, 2 cores per chip</p> <p>TPUv3 - 4 chips, 2 cores per chip</p> <p>https://cloud.google.com/tpu/docs/system-architecture</p> <p>See also generally Norrie et al., “Google’s Training Chips Revealed: TPUs v2 and TPUs v3” (Presented at HotChips Conference, Aug. 2020)</p>

² Unless indicated otherwise, color-coded annotations have been added to the figures in this chart to highlight relevant teachings of the prior art.

'156 PATENT	INFRINGEMENT EVIDENCE
<p>7. A <u>device</u> comprising:</p> <p>at least one first low precision high-dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value,</p> <p>wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=5% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X% of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.05% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input;</p> <p>at least one first computing device adapted to control the operation of the at least one first LPHDR execution unit</p> <p>wherein the at least one first computing device comprises at least one of a central processing unit (CPU), a graphics processing unit (GPU), a field programmable gate array (FPGA), a microcode-based processor, a hardware sequencer, and a state machine; and,</p> <p>wherein the number of LPHDR execution units in the device exceeds by at least one hundred the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide.</p>	<p>As demonstrated below, the Accused Products include multiple components that, separately and independently, meet all the requirements of the claimed “device.” For example, a “TPU Core” satisfies these requirements:</p> <div style="border: 1px solid black; padding: 10px;"> <p>When you request one “Cloud TPU v2” on Google Cloud Platform, you get a virtual machine (VM) which has a PCI-attached TPU board. The TPU board has four dual-core TPU chips. Each TPU core features a VPU (Vector Processing Unit) and a 128x128 MXU (Matrix multiply Unit). This “Cloud TPU” is then usually connected through the network to the VM that requested it. So the full picture looks like this:</p>  <p>Illustration: your VM with a network-attached “Cloud TPU” accelerator. The Cloud TPU itself is made of a VM with a PCI-attached TPU board with four dual-core TPU chips on it.</p> <p>https://codelabs.developers.google.com/codelabs/keras-flowers-convnets/#2</p>  <p>https://cloud.google.com/tpu/docs/system-architecture</p> </div>

'156 PATENT	INFRINGEMENT EVIDENCE
<p>7. A <u>device</u> comprising:</p> <p>at least one first low precision high-dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value, wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=5% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X% of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.05% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input;</p> <p>at least one first computing device adapted to control the operation of the at least one first LPHDR execution unit wherein the at least one first computing device comprises at least one of a central processing unit (CPU), a graphics processing unit (GPU), a field programmable gate array (FPGA), a microcode-based processor, a hardware sequencer, and a state machine; and, wherein the number of LPHDR execution units in the device exceeds by at least one hundred the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide.</p>	 <p>It has two <u>TensorCore</u> Node fabric data and NF controller move on-chip data.</p> <p>Figure 3. TPUv2 chip floor plan.</p> <p>https://cacm.acm.org/magazines/2020/7/245702-a-domain-specific-supercomputer-for-training-deep-neural-networks</p>  <p>Figure 2. Block diagram of a <u>TensorCore</u> (our internal development name for a TPU core, and not related to the Tensor Cores of NVIDIA GPUs).</p> <p><i>Id.</i></p>

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Bfloat16 is a 16-bit floating point representation that provides better training and model accuracy than the IEEE half-precision representation.” <p>https://cloud.google.com/tpu/docs/system-architecture</p> <ul style="list-style-type: none"> “The following figure shows three floating-point[] formats <ul style="list-style-type: none"> fp32 - IEEE single-precision floating-point fp16 - IEEE half-precision floating point bfloat16 - 16-bit <i>brain floating point</i>” <p>https://cloud.google.com/tpu/docs/bfloat16</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th style="text-align: center;">sign</th> <th colspan="7" style="text-align: center;">exponent</th> <th colspan="7" style="text-align: center;">fraction</th> </tr> <tr> <td></td> <td colspan="7" style="text-align: center;">8 bits</td> <td colspan="7" style="text-align: center;">7 bits</td> </tr> </thead> <tbody> <tr> <td>bfloat16 range: ~1e⁻³⁸ to ~3e³⁸</td> <td>S</td> <td>E</td> <td>E</td> <td>E</td> <td>E</td> <td>E</td> <td>E</td> <td>E</td> <td>M</td> <td>M</td> <td>M</td> <td>M</td> <td>M</td> <td>M</td> <td>M</td> </tr> <tr> <td>float32 range: ~1e⁻³⁸ to ~3e³⁸</td> <td>S</td> <td>E</td> <td>E</td> <td>E</td> <td>E</td> <td>E</td> <td>E</td> <td>E</td> <td>M</td> <td>M</td> <td>M</td> <td>M</td> <td>M</td> <td>M</td> <td>M</td> </tr> <tr> <td>float16 range: ~5.9e⁻⁸ to 6.5e⁴</td> <td>S</td> <td>E</td> <td>E</td> <td>E</td> <td>E</td> <td>E</td> <td>M</td> <td>M</td> <td>M</td> <td>M</td> <td>M</td> <td>M</td> <td>M</td> <td>M</td> <td>M</td> </tr> </tbody> </table> <p><i>Id.</i></p> <ul style="list-style-type: none"> “Because general-purpose processors such as CPUs and GPUs must provide good performance across a wide range of applications, they have evolved myriad sophisticated, performance-oriented mechanisms. As a side effect, the behavior of those processors can be difficult to predict, which makes it hard to guarantee a certain latency limit on neural network inference. In contrast, TPU design is strictly minimal and deterministic as it has to run only one task at a time: neural network prediction. You can see its simplicity in the floor plan of the TPU die.” <p>https://cloud.google.com/blog/products/gcp/an-in-depth-look-at-googles-first-tensor-processing-unit-tpu (<i>emphasis in orig.</i>)</p> <ul style="list-style-type: none"> “In mathematics, computer science and physics, a deterministic system is a system in which no randomness is involved in the development of future states of the system. A deterministic model will thus always produce the same output from a given starting condition or initial state.” <p>https://en.wikipedia.org/wiki/Deterministic_system</p> <ul style="list-style-type: none"> For each of the possible valid inputs to the multiplication operation performed by the multipliers within the MXU, Singular has computed the result and compared it to the result of an exact mathematical calculation performed on the same inputs. The results of this test showed that for more than 10% of the possible valid inputs, the numerical value represented by the output signal of each MXU multiplier differs by more than 0.2% from the result of an exact mathematical calculation performed on the same inputs. 	sign	exponent							fraction								8 bits							7 bits							bfloat16 range: ~1e ⁻³⁸ to ~3e ³⁸	S	E	E	E	E	E	E	E	M	M	M	M	M	M	M	float32 range: ~1e ⁻³⁸ to ~3e ³⁸	S	E	E	E	E	E	E	E	M	M	M	M	M	M	M	float16 range: ~5.9e ⁻⁸ to 6.5e ⁴	S	E	E	E	E	E	M	M	M	M	M	M	M	M	M
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<p>7. A device comprising:</p> <p>at least one first low precision high-dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value,</p> <p>wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=5% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X% of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.05% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input;</p> <p>at least one first computing device adapted to control the operation of the at least one first LPHDR execution unit</p> <p>wherein the at least one first computing device comprises at least one of a central processing unit (CPU), a graphics processing unit (GPU), a field programmable gate array (FPGA), a microcode-based processor, a hardware sequencer, and a state machine; and,</p> <p>wherein the number of LPHDR execution units in the device exceeds by at least one hundred the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide.</p>	<ul style="list-style-type: none"> “Each of the cores on a TPU device can <u>execute user computations (XLA ops)</u> independently.” https://cloud.google.com/tpu/docs/system-architecture#pod “TPUs use a VLIW architecture to express instruction-level parallelism to the many compute units of a TensorCore. XLA uses standard VLIW compilation techniques including loop unrolling, instruction scheduling, and software pipelining to keep all compute units busy and to simultaneously move data through the memory hierarchy to feed them.” https://cacm.acm.org/magazines/2020/7/245702-a-domain-specific-supercomputer-for-training-deep-neural-networks/fulltext “The Core Sequencer fetches VLIW (<i>Very Long Instruction Word</i>) instructions from the core's on-chip, software-managed Instruction Memory (Imem), executes scalar operations using a 4K 32-bit scalar data memory (Smem) and 32 32-bit scalar registers (Sregs), and forwards vector instructions to the VPU. The 322-bit VLIW instruction can launch eight operations: two scalar, two vector ALU, vector load and store, and a pair of slots that queue data to and from the matrix multiply and transpose units. The XLA compiler schedules loading Imem via independent overlays of code, as unlike conventional CPUs, there is no instruction cache.” <i>Id.</i> “The Vector Processing Unit (VPU) performs vector operations using a large on-chip <i>vector memory (Vmem)</i> with 32K 128 x 32-bit elements (16MiB), and 32 2D <i>vector registers (Vregs)</i> that each contain 128 x 8 32-bit elements (4 KiB). The VPU streams data to and from the MXU through decoupling FIFOs. The VPU collects and distributes data to Vmem via data-level parallelism (2D matrix and vector functional units) and instruction-level parallelism (8 operations per instruction).” <i>Id.</i> <p>The diagram illustrates the internal architecture of a TensorCore. It features a central 'TensorCore' block, which contains a 'Core Sequencer' (highlighted with a red border) and a 'Vector Unit (VPU)'. The 'Core Sequencer' is connected to 'Matrix Multiply (MXU)' and 'Transpose Permute Unit' blocks. The 'VPU' is also connected to these units. External components include 'Host Queues (over PCIe)', 'HBM Memory (8/16 GiB)', and an 'Interconnect Router (ICI)'. Bidirectional arrows indicate communication between the Host Queues and the HBM Memory, between the HBM Memory and the TensorCore, and between the TensorCore and the Interconnect Router.</p> <p>Figure 2. Block diagram of a TensorCore (our internal development name for a TPU core, and not related to the Tensor Cores of NVIDIA GPUs).</p>

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